

Hyperband television tuner

KS-H-148 E

FEATURES

- Member of the KS-H-130/140 family small sized VHF/Hyperband/UHF tuner
- Systems CCIR: B/G, H, L, L', I, I'; OIRT: D/K
- Digitally controlled (PLL) tuning via I²C-bus
- Fast 400kHz I²C-bus protocol compatible with 3.3V and 5V micro controllers
- Off-air channels, S-cable channels and Hyperband
- World standardized mechanical dimensions and world standard pinning
- Weak signal booster (I2C controlled switch able gain amplifier)
- Low power
- Compact size
- Various connector types available

The IF output can drive a SAW filter directly and has capability to drive an symmetrical or asymmetrical load.

The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- CISPR 13 (1990), including amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner or printed directly on the top cover:

- Company logo
- Type number
- Year and month code
- Quality inspection print

DESCRIPTION

The KS-H-148 E tuner belongs to the KS-H-130/140 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF/Hyperband/UHF tuner suitable for CCIR systems B/G, H, L, L', I, I' and OIRT systems D/K. A weak signal booster can be activated through the bus to increase the overall gain of the tuner to improve TV reception in case of weak signal strength.

ORDERING INFORMATION

TYPE	SYSTEM	DESCRIPTION
KS-H-148 E	CCIR	Symmetrical IF, IEC connector (14.5 mm), I ² C status byte, vertical mount
KS-H-148 DE	CCIR	Symmetrical IF, IEC connector (14.5 mm), I ² C status byte, horizontal mount
KS-H-148 EA	CCIR	Asymmetrical IF, IEC connector (14.5 mm), I ² C status byte, vertical mount
KS-H-148 EAL	CCIR	Asymmetrical IF, IEC connector (19.0 mm), vertical mount
KS-H-148 DEA	CCIR	Asymmetrical IF, IEC connector (14.5 mm), I ² C status byte, horizontal mount

				ABA2.222.148 ETS	Pages
Correct.	Doc. №	Signature	Date		
Prepared	G. Jurna		05.06.16		12
Confirmed	D. Liksiene		05.06.16		

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INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY (MHz)				
	SYSTEM B/G, H	SYSTEM L	SYSTEM L'	SYSTEM I	SYSTEM I'
Picture carrier	38.90	38.90	33.40	39.50	38.90
Color	34.47	34.47	37.83	35.07	34.47
Sound 1	33.40	32.40	39.90	33.50	32.90
Sound 2	33.16	-	-	33.00	32.40

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

Type	BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
		CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
KS-H-148 E	Low band	E2 to Z	48.25 to 83.25 ⁽¹⁾	S01 to S08	69.25 to 154.25
	Mid band	E5 to E12	175.25 to 224.25	S09 to S38	161.25 to 439.25
	High band	E21 to E69	471.25 to 855.25 ⁽²⁾	S39 to S41	447.25 to 463.25

Notes

1. Enough margin is available to tune down to 45.25 MHz.
2. Enough margin is available to tune up to 863.25 MHz.

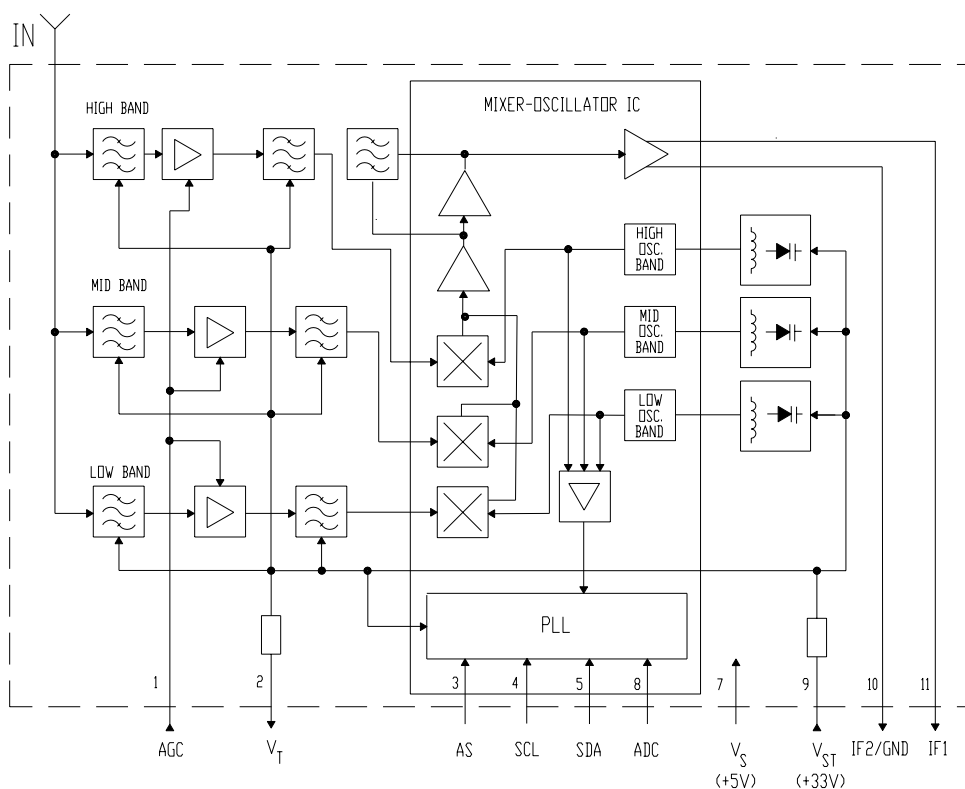


Fig.1 Electrical block diagram

Hyperband television tuner
KS-H-148 E
PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	Gain control voltage
V _T	2	KS-H-148 E/DE/EA/DEA: tuning voltage, KS-H-148 EAL: not connected
AS	3	I ² C-bus address select
SCL	4	I ² C-bus serial clock
SDA	5	I ² C-bus serial data
n.c.	6	Not connected
V _S	7	Supply voltage +5 V
ADC	8	KS-H-148 E/DE/EA/DEA: ADC input, KS-H-148 EAL: not connected
V _{ST}	9	Tuning supply voltage +33 V
IF2	10	KS-H-148 E: symmetrical IF output, KS-H-148 EA: ground
IF1	11	KS-H-148E: symmetrical IF output, KS-H-148 EA: asymmetrical IF output
GND	MT1 – MT4	Mounting tags (ground)
IN		Aerial input connector KS-H-148 E/DE/EA/DEA: IEC (14.5 mm), KS-H-148 EAL: IEC (19.0 mm)

LIMITING VALUES
Environmental conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Non-operational conditions				
T _{amb}	Ambient temperature	-40	+60	°C
RH	Relative humidity	-	100	%
Operational conditions				
T _{amb}	Ambient temperature	-15	+60	°C
RH	Relative humidity	-	93	%

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Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
V_S	Supply voltage	7	4.75	5.00	5.5	V
I_S	Supply current		-	65	110	mA
V_{ST}	Supply voltage	9	30	33	35	V
I_{ST}	Supply current		-	-	1.7	mA
V_{AGC}	AGC input voltage	1	-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range		0.3	-	4.0	V
I_{AGC}	AGC input current		-	-	20	μA
V_{AS}	Address select input voltage	3	-	-	5.5	V
V_{SCL}	Serial clock input voltage	4	-	-	5.5	V
V_{SDA}	Serial data input voltage	5	-	-	5.5	V
I_{SDA}	Serial data input current		-1	-	5	mA

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related to systems B, G and H.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	Ambient temperature	25 +/- 5	$^{\circ}C$
RH	Relative humidity	60 +/- 15	%
V_S	Supply voltage	5.0 +/- 0.1	V
V_{AGC}	AGC input voltage	4.0 +/- 0.1	V
V_{ST}	Tuning supply voltage	33 +/- 0.5	V
t_{pr}	Pre-heating time (+5 V at pin 7)	10	minute
$Z_{S(AE)}$	Aerial source impedance (unbalanced)	75	Ω

Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VSWR	Reflection coefficient	Referred to 75 Ω impedance	-	2	4	
V_{ant}	Antenna connection disturbance voltage	< 1.75 GHz; comply to "EN55013 section 3.3"	-	-	46	dB μV

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General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_b	Frequency range: low band mid band high band		48.25 161.25 447.25	- - -	154.25 439.25 855.25	MHz MHz MHz
Y	RF-curves, tilt (the difference from the top of the curve to the corresponding carrier): 38.9 MHz and 33.4 MHz 32.4 MHz	The IF output is loaded with a test circuit according diagram fig.2	- -	2.5 3.5	4.0 5.0	dB dB
G_v	Voltage gain: all channels gain taper	The IF output is loaded with a test circuit according diagram fig.2	40 -	45 -	52 7	dB dB
ΔG_v	Gain increase when weak signal booster mode is activated: KS-H-148 EA KS-H-148 E	The IF output is loaded with a test circuit according diagram fig.2	- -	10 16	- -	dB dB
F	Noise: low band mid band high band	The IF output is loaded with a test circuit according diagram fig.2	- - -	6 6 6	9 9 8	dB dB dB
ΔV_{AGC}	AGC input voltage range (0.5-4.0V): low and mid band high band		45 40	55 50	- -	dB dB
α_i	Image rejection: low band mid band, <300 MHz mid band, >300 MHz high band		66 60 56 50	70 69 64 60	- - - -	dB dB dB dB
α_{IF}	IF rejection (picture): channel E2 low, mid and high bands		65 ¹⁾ 70	70 80	- -	dB dB
m_x	Cross modulation: in-band low band (n+/-2) mid band (n+/-2) high band (n+/-2) out of band			80 74 74	- - - -	dB μ V dB μ V dB μ V dB μ V
	Overloading: 1 dB gain compression PLL lock-out			75 100	- -	dB μ V dB μ V
	Residual carrier FM caused by I2C bus cross talk		-	5		kHz
	Oscillator characteristics: oscillator tuning resolution lock-in time		- -	- -	note 2 150	kHz msec
V_{ESD}	Electrostatic discharge (ESD): protection on pins 1 to 5 and 7 to 11 protection on antenna socket	note 3	2 8	- -	- -	kV kV

Notes

1. Channel E2 56 dB min.
2. Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see Table "Ratio select bits").
3. The tuner meets specifications IEC 1000-4-2 level 1 for pins and level 4 for antenna socket.

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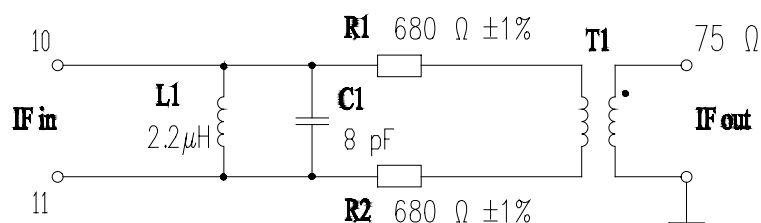
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Visibility test

The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.



Dummy Attenuation = 22.6 dB

T1 – RF Transformer.

W – Ratio = 1:4 (IF – IN = 4 / IF – OUT = 1).

Type: MCL T4-1 or equivalent.

Supplier: Industrial Electronics GmbH,
Hauptstr. 71-79,
65760 Eschborn, Tel: (0)6196 - 48689

Fig. 2 Test circuit.

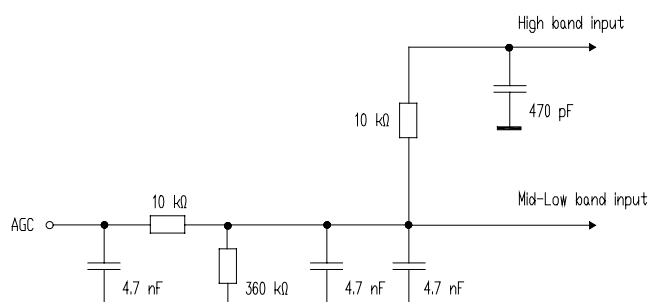


Fig.3 Internal AGC circuit.

Recommended adjustment of Tuner AGC in TV chassis:

Channel: S39 (447.25 MHz PC-frequency)

Input level: 70 dB μ V/75 Ω

IF output level: 105 dB μ V

Gain reduction: 10 dB

AGC-Voltage: 2.20 V +/-0.2V

AGC characteristics shown on Fig. 6

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APPLICATION INFORMATION

WRITE mode

BYTE	BITS								
	7 ⁽¹⁾ MSB	6	5	4	3	2	1	0 LSB	A ⁽²⁾
Address byte	1	1	0	0	0	MA1	MA2	R/W ⁽³⁾	A
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte	1	CP	T2	T1	T0	RSA	RSB	WSB	A
Band-switch byte	X	X	X	BS4	BS3	BS2	BS1	BS0	A

Notes

1. X = don't care.
2. A = Acknowledge.
3. R/W bit = 0 for WRITE mode, R/W bit = 1 for READ mode.

Address selection

$V_s = 5\text{ V}$ (PLL supply voltage).

MA1	MA0	ADDRESS	VOLTAGE AT PIN 3
0	0	C0	0 V to $0.1xV_s$
0	1	C2	Open or $0.2xV_s$ to $0.3xV_s$
1	0	C4	$0.4xV_s$ to $0.6xV_s$
1	1	C6	$0.9xV_s$ to $1.0xV_s$

Programmable divider settings (bytes 1 and 2)

$$\begin{aligned}
 f_{\text{OSC}} &= f_{\text{DIV}} \times N, & f_{\text{OSC}}: & \text{locked oscillator frequency,} \\
 f_{\text{DIV}} &= f_{\text{OSC}}/N (=f_{\text{REF}} \text{ when PLL is locked}), & N: & \text{programmable divider ratio,} \\
 f_{\text{REF}} &= 4\text{ MHz/RD}, & \text{RD:} & \text{reference divider.}
 \end{aligned}$$

Divider ratio:

$$N = (16384 \times n14) + (8192 \times n13) + (4096 \times n12) + (2048 \times n11) + (1024 \times n10) + (512 \times n9) + (256 \times n8) + (128 \times n7) + (64 \times n6) + (32 \times n5) + (16 \times n4) + (8 \times n3) + (4 \times n2) + (2 \times n1) + n0$$

CONTROL BYTE

Charge pump current control bit

CP can be set to either 0 (low current, 20 μA) or 1 (high current, 100 μA , at power-on).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Unnecessary charge pump action will result in very low tuning voltage ($V_T = 0\text{V}$), which may drive the oscillator to extreme conditions.

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Test mode setting bits

T2	T1	T0	Setting
0	0	0	normal mode
0	0	1	normal mode ⁽¹⁾
0	1	0	charge pump OFF
0	1	1	band-switch byte ignored
1	1	0	charge pump ON; sinking current
1	1	1	charge pump ON; sourcing current
1	0	0	internal test mode
1	0	1	internal test mode

Note

1. This is the default mode at power-on reset.

Ratio select bits

RSA	RSB	REFERENCE DIVIDER	STEP SIZE (kHz)
X	0	80	50.00
0	1	128	31.25
1	1	64	62.50

Weak Signal Booster control bit

WSB=0, normal mode - no gain increase, IF filter is used.

WSB=1, Weak Signal Booster activated, IF filter is by-passed.

BAND-SWITCH BYTE

BIT								ACTIVE PORT	BAND
X MSB	X	X	BS4	BS3	BS2	BS1	BS0 LSB		
X	X	X	0	0	0	0	1	BS0	Low band
X	X	X	0	0	0	1	0	BS1	Mid band
X	X	X	0	0	1	0	0	BS2	High band

READ mode

BYTE	BITS								
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR ⁽²⁾	FL ⁽³⁾	1	1	1	A2 ⁽⁴⁾	A1 ⁽⁴⁾	A0 ⁽⁴⁾	A

Notes

1. A = Acknowledge.
2. POR = Power On Reset flag (POR=1 at power on).
3. FL = In-lock flag (FL=1 at loop is phase-locked).
4. A2, A1, and A0 are the digital outputs of the 5 level ADC.

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ADC BYTE

VOLTAGE AT PIN 8	A2	A1	A0
$0.60 \times V_S$ to V_S	1	0	0
$0.45 \times V_S$ to $0.60 \times V_S$	0	1	1
$0.30 \times V_S$ to $0.45 \times V_S$	0	1	0
$0.15 \times V_S$ to $0.30 \times V_S$	0	0	1
0 to $0.15 \times V_S$	0	0	0

Note

1. Accuracy is $\pm 0.03 \times V_S$.

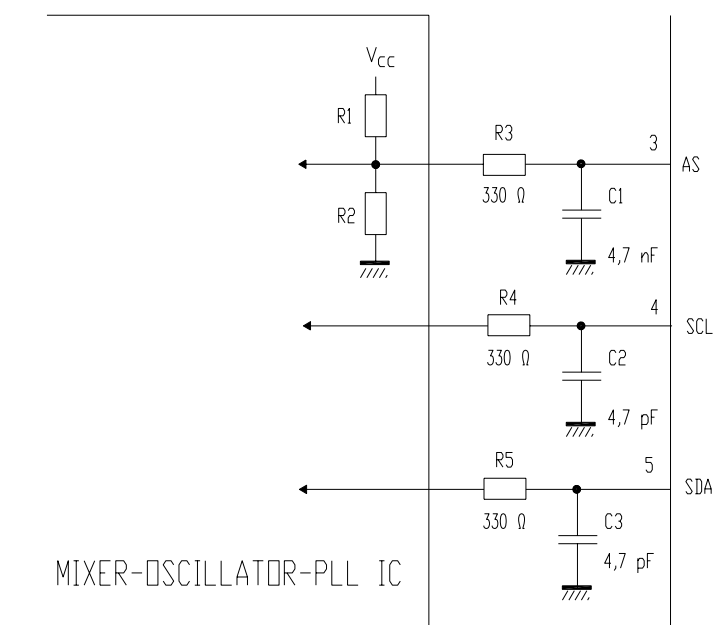


Fig.4 I²C-bus load.

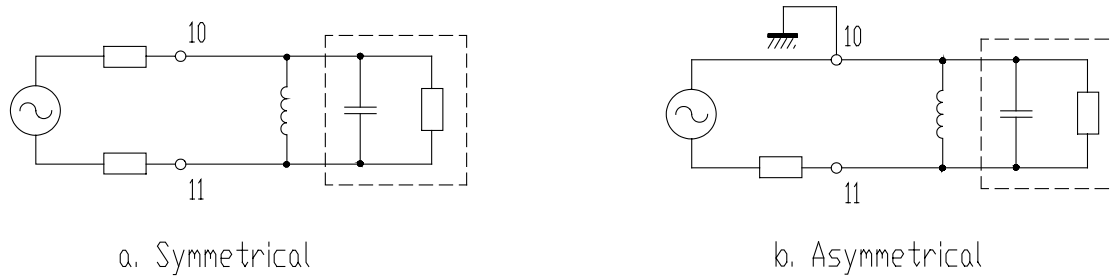


Fig.5 IF loading using SAW filters.

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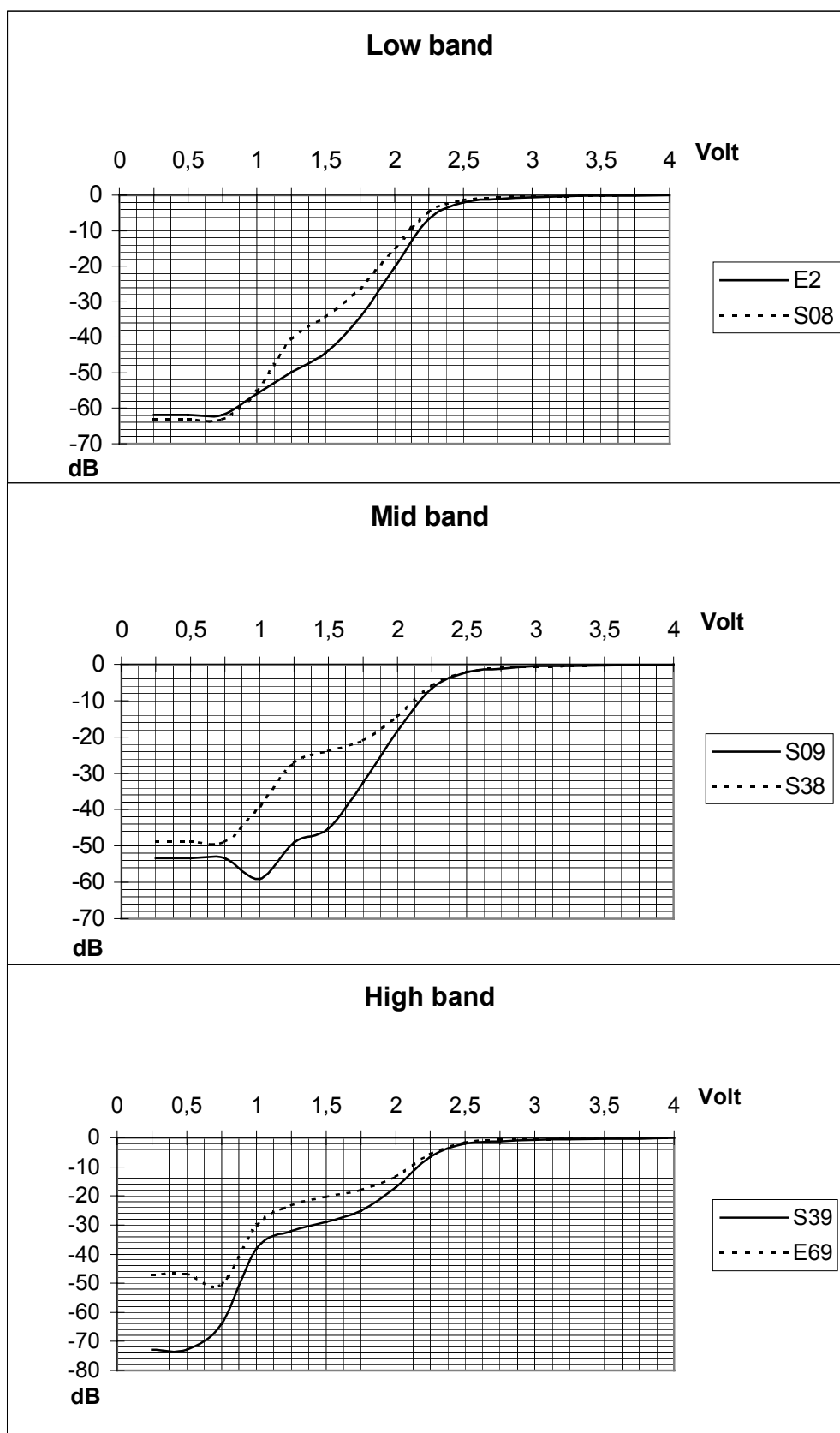


Fig.6 AGC characteristics.

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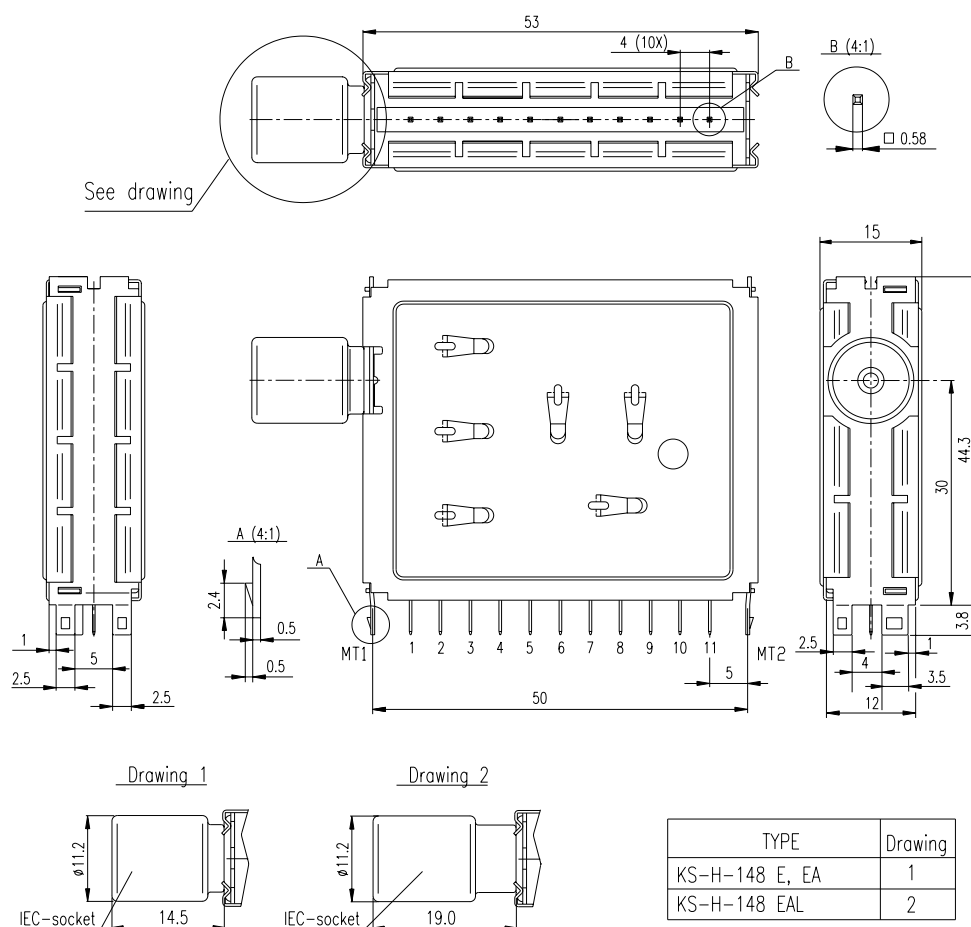
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Fig.7 Mechanical outline. Vertical mounting

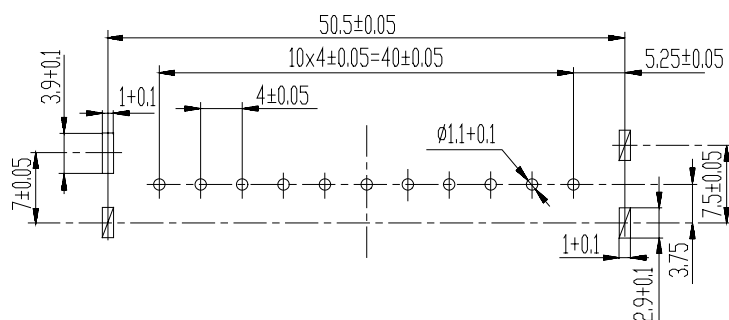


Fig.8 Punching pattern seen from solder side. Vertical mounting

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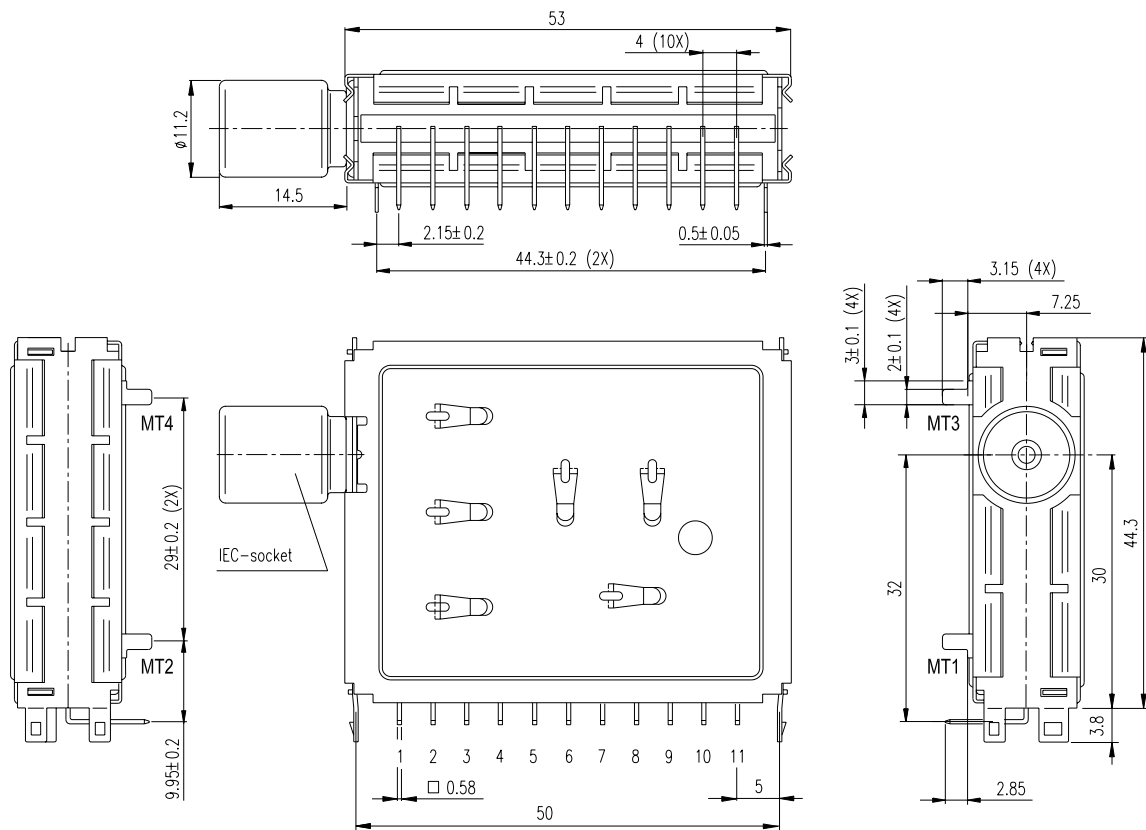


Fig.9 Mechanical outline. Horizontal mounting

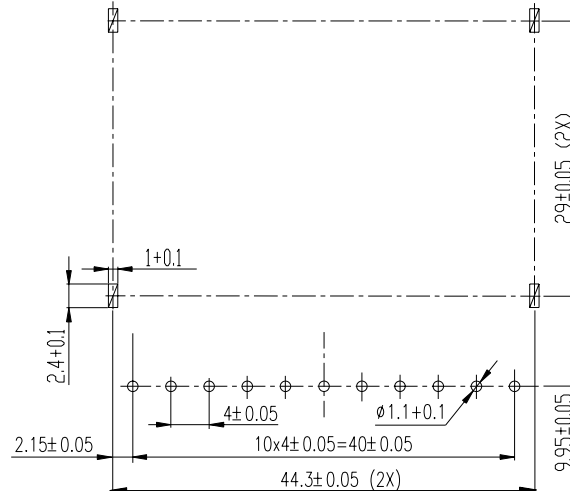


Fig.10 Punching pattern seen from solder side. Horizontal mounting

Aerial connections

Standard IEC or phono sockets female 75 Ω.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Selteka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Selteka for any damages resulting from such improper use or sale.