UV1316 MK4

VHF/UHF/Hyperband PAL TV tuner

Rev.o — 04.07.2007 Product data sheet

1. General description

The UV1316 MK4 tuner belongs to the UV1300 family of fourth generation WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The UV1316 MK4 is backwards compatible with its predecessors, the UV1316 MK1, MK2 and Mk3. In addition, a 5 level Analog Digital converter comes standard with the MK4.

This tuner complies with the requirements of radiation, signal handling capability and immunity conforming to:

- CISPR 13 (1990) included amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020
- CISPR 13 (4th edition)

Table 1. Intermediate frequencies

SIGNAL	Frequency (MHz) [1]				
	System B/G, H	System L	System L' [2]	System I	System I'
Picture carrier	38.90	38.90	33.40	39.50	38.90
Colour	34.47	34.47	37.83	35.07	34.47
Sound 1	33.40	32.40	39.90	33.50	32.90
Sound 2	33.16	-	-	33.00	32.40

[1] The oscillator frequency is above the input signal frequency

[2] Does not cover channel FA

Table 2. Channel coverage

Band	Channels	Frequency range (MHz)
Off-air channels		
Low band	E2 to C	48.25 to 82.25 [1]
Mid band	E5 to E12	175.25 to 224.25
High band	E21 to E69	471.25 to 855.25 [2]
Cable channels		
Low band	S01 to S08	69.25 to 154.25
Mid band	S09 to S38	161.25 to 439.25
High band	S39 to S41	447.25 to 463.25

[1] Sufficient margin is available to tune down to 44.00 MHz.

[2] Sufficient margin is available to tune up to 865.25 MHz.

2. Features

- Member of UV1300 MK4 family of small-sized full band tuners
- Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
- Digitally-controlled (PLL) tuning via I^2C-bus
- Reduced power consumption
- Software controlled weak signal booster
- Off-air, S-cable and hyperband channels from 48.25 MHz to 863.25 MHz inclusive
- World standardized mechanical dimensions and pinning, horizontal mounting is optionally available
- Various connector types available

3. Applications

- Terrestrial tuner

4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
UV1316/A I-4	3139 147 20691	Asymmetrical IF; IEC connector	-
UV1316/S I-4	3139 147 20891	Symmetrical IF; IEC connector	-
UV1316/A I H-4	3139 147 22101	Asymmetrical IF; IEC connector, Horizontal mount	-
UV1316/S I H-4	3139 147 22111	Symmetrical IF; IEC connector, Horizontal mount	-
UV1316/A L-4	3139 147 22301	Asymmetrical IF; IEC long connector	-
UV1316/A P-4	3139 147 22411	Asymmetrical IF; Phono connector	-
UV1316/A L H-4	3139 147 22421	Asymmetrical IF; IEC long connector, Horizontal mount	-
UV1316/S L-4	3139 147 24111	Symmetrical IF; IEC long connector	-
UV1316/A D H-4	3139 147 24721	Asymmetrical IF; Long IEC connector, Horizontal mount	-

5. Marking

The following information is printed on a sticker that is on the top cover of the tuner.

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code

6. Block diagram

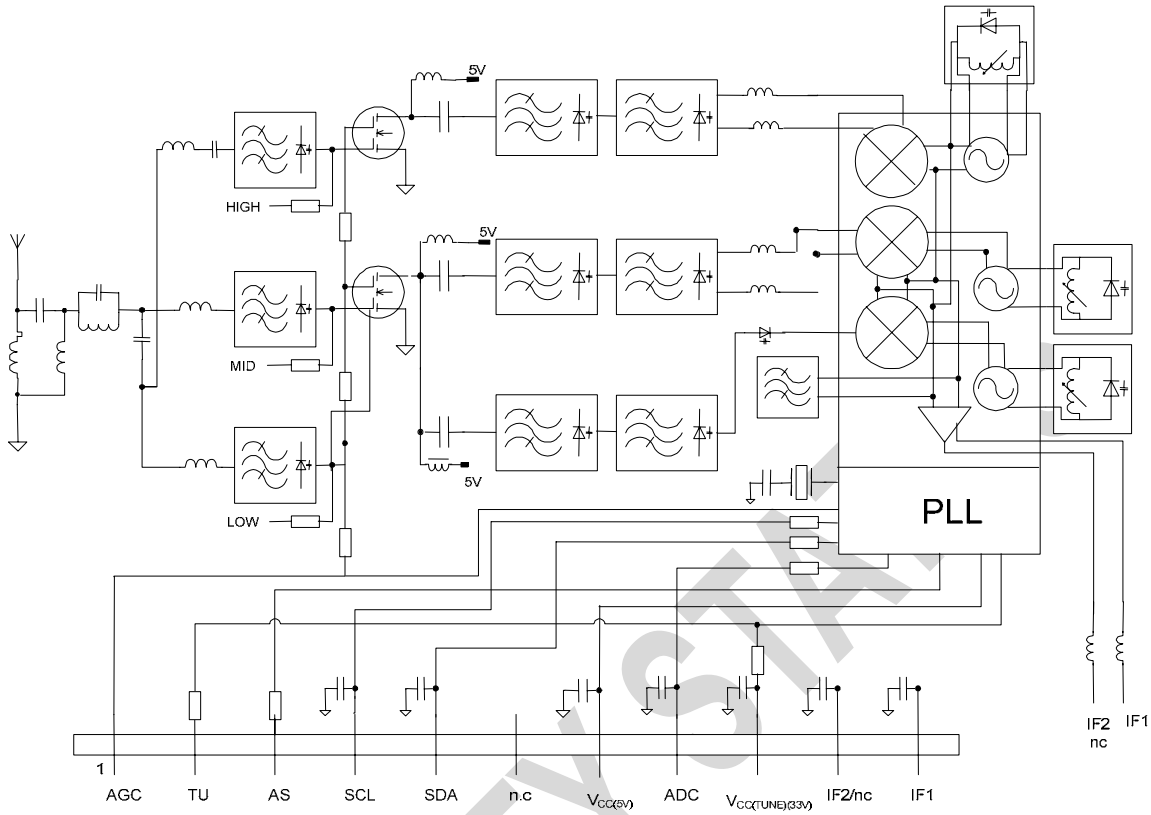

Fig 1. Block diagram

7. Pinning information

Table 4. Pin description

Pin name	Pin	Description
AGC	1	Automatic gain control voltage
TU	2	Tuning voltage output monitor
AS	3	I^2C-Bus address select
SCL	4	I^2C-Bus clock input
SDA	5	I^2C-Bus data input and output
n.c	6	Not connected
$V_{CC(5V)}$	7	Supply voltage (5 V)
ADC	8	ADC input [1]

Pin name	Pin	Description
$V_{CC(TUNE)(33V)}$	9	Tuning supply voltage (33 V)
IF2/nc	10	IF output 2 (symmetrical) / not connected (asymmetrical)
IF1	11	IF output (asymmetrical) / IF output 1 (symmetrical)
GND	M1, M2, M3, M4	Mounting tags (ground)

[1] Standard 5 level ADC

8. Limiting values

Table 5. Limiting values

Environmental conditions

Symbol	Parameter	Conditions	Min	Max	Unit
Non-operational Conditions					
T_{amb}	ambient temperature		−25	+85	°C
RH	relative humidity		-	95	%
g_B	bump acceleration	25 g	-	245	m/s^2
g_S	shock acceleration	50 g	-	490	m/s^2
	vibration amplitude	10 Hz to 55 Hz	-	0.35	mm
Operational Conditions					
T_{amb}	Ambient temperature		−10	+65	°C
RH	Relative humidity		-	95	%

Table 6. Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions.

Symbol	Parameter	Pin		Min	Typ	Max	Unit
$V_{CC(5V)}$	Supply voltage (5 V)	7		4.75	5.00	5.50	V
$V_{ripple(p\_p)}$	Peak to peak ripple voltage susceptibility		[1]	10	-	-	mV_{PP}
$I_{CC(5V)}$	Supply current (5 V)			-	-	100	mA
$V_{CC(TUNE)(33V)}$	Tuning supply voltage (33 V)	9		30	33	35	V
$V_{ripple(p\_p)}$	Peak to peak ripple voltage susceptibility			10	-	-	mV
$I_{CC(TUNE)(33V)}$	Tuning supply current (33 V)			-	-	1.7	mA
V_{AGC}	AGC input voltage	1		-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range			0.5	-	4.0	V

Symbol	Parameter	Pin	Min	Typ	Max	Unit
I_{AGC}	AGC input current		-	-	20	μA
V_{AS}	voltage on pin AS	3	-	-	5.5	V
V_{SCL}	voltage on pin SCL	4	−0.3	-	5.5	V
V_{SDA}	voltage on pin SDA	5	−0.3	-	5.5	V
I_{SDA}	current on pin SDA		−1	-	5	mA

[1] Sinusoidal ripple voltage superimposed on the 5 V supply voltage in the frequency range of 15 kHz to 500 kHz. Criteria for TV interference is >57 dB

9. Static Characteristics

9.1 Electrical performance

Unless otherwise specified, all electrical values apply at the following conditions and the electrical performance is related to system B, G and H.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions

Table 7. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	Ambient temperature		-	25 ± 5	-	°C
RH	Relative humidity		-	60 ± 15	-	-
$V_{CC(5V)}$	Supply voltage (5 V)		-	5 ± 0.125	-	V
V_{AGC}	AGC input voltage		-	4 ± 0.1	-	V
$V_{CC(TUNE)(33V)}$	Tuning supply voltage (33 V)		-	33 ±0.5	-	V
t_{pr}	Pre-heating time	5 V at pin 7	-	10	-	mins
$Z_{S(AE)}$	Aerial source impedance	unbalanced	-	75	-	Ω

10. Dynamic Characteristics

Table 8. Antenna input characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VSWR	Reflection coefficient referred to 75 Ω	Picture carrier at maximum gain	-	5	-
V_{ant}	Antenna connection disturbance voltage	< 950 MHz	-	46	dBμV
		0.950 < f < 2.15 GHz	-	54	dBμV

Table 9. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_b	Frequency range					
	Low band		48.25	-	154.25	MHz
	Mid band		161.25	-	439.25	MHz
	High band		447.25	-	855.25	MHz
Δf_b	Frequency margin					
	Low band end	negative	−2	-	+3	MHz
	Mid band		−3	-	+3	MHz
	High band		−3	-	+3	MHz
G_V	Voltage gain					
	Low band		40	45	-	dB
	Mid band		40	45	-	dB
	High band		40	45	-	dB
	Gain taper	off-air channels	-	-	8	dB
NF	Noise figure					
	Low band		-	5	9	dB
	Mid band		-	5	9	dB
	High band		-	5	9	dB
$\Delta V_{i(AGC)}$	AGC input voltage range					
	Low band		40	50	-	dB
	Mid band		40	50	-	dB
	High band		35	45	-	dB
α_{image}	Image rejection (nominal gain to 10 dB gain reduction)					
	Low band		66	75	-	dB
	Mid band	< 300 MHz	66	75	-	dB
		> 300 MHz	60	78	-	dB
	High band		50	55	-	dB
α_{IF}	IF rejection	picture	60	80	-	dB
$X_{IF/2}$	½ IF susceptibility		60	80	-	dBμV
$\alpha_{RF/2}$	½ RF rejection		60	-	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_S	Sound-chroma moire rejection					
	Off-air	up to 40 dB gain reduction	56	65	-	dB
	UHF	up to 30 dB gain reduction	56	75	-	dB
X_{mod}	Cross modulation					
	All band (n ±1)	in band	66	-	-	dBμV
	Low band (n ±2)	in band	70	82	-	dBμV
	Mid band (n ±2)	in band	70	82	-	dBμV
	High band (n ±2)	in band	68	80	-	dBμV
	Out of band		-	100	-	dBμV
V_{OSC}	Oscillator voltage					
	IF pin		-	70	85	dBμV
	All other pins		-	50	70	dBμV
Overloading						
	1 dB gain compression		74	81	-	dBμV
	PLL lock-out		90	-	-	dBμV
Tuning system interference						
Crystal harmonics interference rejection at IF output		input level 50 dBμV	54	-	-	dB
Divider interference rejection at IF output			57	-	-	dB
Residual FM caused by I^2C cross-talk			-	-	5	kHz
Electrostatic discharge voltage		on all pins [1]	2	-	-	kV
Surge protection voltage		on antenna	4	-	-	kV
Oscillators						
Oscillator tuning resolution		[2]	31.25	-	-	kHz
lock-in time			-	-	100	msec

[1] All the pins of the tuner are protected against electrostatic discharge (ESD) up to 2 kV. The product is in accordance with EIA / JES 022-A114-A

[2] Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see table “Ratio select bits”)

10.1 Amplitude response

The tilt of the response curve is defined as the difference from the top of the corresponding picture or sound carriers

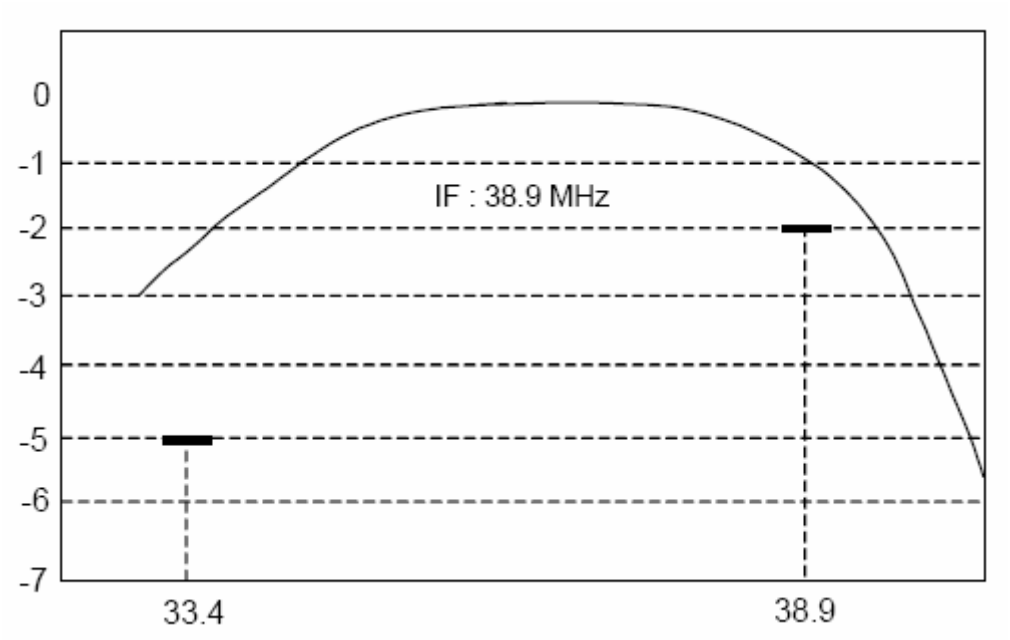

Fig 2. Amplitude response curve (tilt)

10.2 Visibility test (input immunity and immunity from radiated fields)

The tuners meet the requirements of the European Standard "*EN55020*", when measured in an adequate television receiver [1]. The external AGC must be adjusted so that the picture carrier level (top sync) at the tuner output does not exceed 107 dBμV at an input signal level of 74 dBμV or greater.

1. Or measured in our reference application board.

10.3 Radiation

The tuners meet the requirements of the European Standard "*EN55013*" and "CISPR13" (1990), when measured in an adequate television receiver [1].

11. Application information

11.1 Write mode

A detailed description of the I²C-Bus specification with applications is given in brochure The I²C-Bus and how to use it. This brochure may be ordered using the code number 9398 393 40011.

Table 10. I²C-Bus data format

Name	Byte	Bits								ACK
		MSB							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	$R/\overline{W}$ =0	A
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	WSB	A
Band switch byte	BB	X	X	X	P4	P3	P2	P1	P0	A

Description of symbols used

Symbol	Description	
ACK	Acknowledge	
MA1, MA0	Programmable address bits see Table 11	
$R/\overline{W}$	Logic 0 for write mode	
N14 to N0	Programmable divider bits	N = N14 x 2^{14} + N13 x 2^{13} + …+ N1 x 2^{1} + N0
CP	Charge pump current control bit	Logic 0 : charge pump current is 20 μA
		Logic 1 : charge pump current is 100 μA
T2, T1, T0	Test bits (see Table 12)	
RSA, RSB	reference divider ratio select bits (see Table 13)	
WSB	Weak signal booster control bit	Logic 0 : normal mode, no gain increase, IF filter is used
		logic 1 : weak signal booster activated, IF filter is by-passed
P0 to P4	ports control bits	Logic 0 : corresponding port is ‘OFF’, high impedance state (default)
		Logic 1 : corresponding port is ‘ON’.

Table 11. I^2C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage on the AS input. The relationship between MA1 and MA0 and the input voltage applied to the AS input

Voltage applied on AS input	Address	MA1	MA0
0 V to 0.1 V x V_{CC}	C0	0	0
Open or 0.2 V x V_{CC} to 0.3 V x V_{CC}	C2	0	1
0.4 V x V_{CC} to 0.6 V x V_{CC}	C4	1	0
0.9 V x V_{CC} to 1.0 V x V_{CC}	C6	1	1

Table 12. Test modes

T2	T1	T0	Test mode
0	0	0	normal mode
0	0	1	normal mode [1]
0	1	0	charge pump is “OFF” [2]
0	1	1	byte BB ignored
1	1	0	charge pump is sinking current
1	1	1	charge pump is sourcing current
1	0	0	½ f_{REF} is available on port P3 [3]
1	0	1	½ f_{DIV} is available on port P3 [3]

[1] This is the default mode at power-on reset

[2] ½ f_{REF} is available on port P3

[3] The P3 port cannot be used when these test modes are active

Table 13. Reference divider ratio select bits

Crystal frequency or signal at XTIN of 4 MHz

Step size	Reference divider ratio	RSA	RSB
50.0 kHz	80	X	0
31.25 kHz	128	0	1
62.5 kHz	64	1	1

Table 14. Control byte

Port 0 to 3 control the band switching

Band switching	0	0	0	P4	P3	P2	P1	P0
Low band	0	0	0	0	0	0	0	1
Mid band	0	0	0	0	0	0	1	0
High band	0	0	0	0	0	1	0	0

11.2 Telegram examples

Start – ADB – ACK – DB1 – ACK – DB2 – ACK – stop
Start – ADB – ACK – CB – ACK – – BB – ACK – stop
Start – ADB – ACK – CB – ACK – stop
Start – ADB – ACK – DB1 – ACK – DB2– ACK – CB – ACK – BB – ACK – stop
Start – ADB – ACK – CB – ACK – BB– ACK – DB1 – ACK – DB2 – ACK – stop
Start – ADB – ACK – DB1 – ACK – DB2– ACK – CB – ACK – stop

Note:

Start	= start condition
ADB	= address byte
ACK	= Acknowledge
DB1	= divider byte 1
DB2	= divider byte 2
CB	= control byte
BB	= band-switch byte
Stop	= stop condition

For channel selection involving band switching, in order to ensure smooth tuning to the desired channel without causing unnecessary charge pump action, it is recommended to consider the difference between wanted channel frequency (fw) and the current channel frequency (fc).

- If fw > fc, use telegram as

  Start – ADB – ACK - DB1 – ACK – DB2 – ACK - CB – ACK - BB – ACK – Stop

- If fw < fc, use telegram as

  Start – ADB – ACK - CB – ACK – BB – ACK - DB1 – ACK - DB2 – ACK – Stop

Unnecessary charge pump action will result in very low tuning voltage ($V_T \approx 0$ V) which may drive the oscillator to extreme conditions.

11.2.1 Read mode

Data can be read from the device by setting R/W bit to 1. After the slave address has been recognized, the device generates an Acknowledge pulse and the first DATA byte (status byte) is transferred on the SDA line (MSB first). DATA is valid on the SDA line during a HIGH-level of the SCL clock signal. A second DATA byte can be read from the device if the microcontroller generates an Acknowledge on the SDA line (master Acknowledge). End of transmission will occur if no master Acknowledge occurs. The device will then release the DATA line to allow the microcontroller to generate a STOP condition.

The POR flag is set to 1 at power-on. The flag is reset when an end-of-data is detected by the device (end of a READ sequence). Control of the loop is made possible with the in-LOCK flag FL which indicates when the loop is locked (FL=1).

The internal AGC status can be known from bit AGC (AGC=1), which indicates when the selected take-over point is reached

A built-in ADC is available on the P6/ADC pin. This converter can be used to apply AFC information to the microcontroller from the IF section of the television. The relationship between the bits A2, A1 and A0 is given in Table 16

Table 15. Read data format

Name	Byte	Bits							
		MSB [1]							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	$R/\overline{W}$ =1
Status byte	SB	POR	FL	1	1	1	A2	A1	A0

[1] MSB is transmitted first.

Description of symbols used

Symbol	Description	
MA1, MA0	Programmable address bits (see Table 11)	
$R/\overline{W}$	Logic 1 for read mode	
POR	Power-on reset flag	logic 0 : after end of the first read sequence
		logic 1 : at power-on
FL	In-lock flag	logic 0 : loop is not locked
		logic 1 : loop is locked
A2, A1, A0	Digital output of the 5 level ADC	

Table 16. ADC digital outputs

Accuracy is ±0.03 x V_{CC}, no erratic codes in the transition

A2	A1	A0	Voltage applied on ADC input
1	0	0	0.6 V x V_{CC} to 5.5 V
0	1	1	0.45 V x V_{CC} to 0.6 V x V_{CC}
0	1	0	0.30 V x V_{CC} to 0.45 V x V_{CC}
0	0	1	0.15 V x V_{CC} to 0.30 V x V_{CC}
0	0	0	0 V to 0.15 V x V_{CC}

11.2.1.1 Telegram examples

Start – AB (R/W=1) – $XX^{(1)}$ – $X^{(2)}$ – Stop
Start – AB (R/W=1) – $XX^{(1)}$ – ACK – $XX^{(1)}$ – $X^{(2)}$ - Stop

(1) XX = Read status byte

(2) X = No Acknowledge from the master means end of sequence

11.3 Power-on-reset

The power-on detection threshold voltage VPOR is set to tbf V at room temperature. Below this threshold the device is reset to the power-on state.

At power-on state the following actions take place

- The charge pump current is set to 100 μA
- The test bits T2, T1 and T0 are set to logic ‘001’. The charge pump can be either sinking or sourcing
- The weak signal booster is disabled

- All ports are off and the high band is selected by default

Table 17. Default setting of the bits at power-on-reset

Name	Byte	Bits							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	X
Divider byte 1	DB1	0	X	X	X	X	X	X	X
Divider byte 2	DB2	X	X	X	X	X	X	X	X
Control byte	CB	1	1	1	1	0	X	X	0
Band switch byte	BB	X	X	X	0	0	0	0	0

11.4 Tuning supply voltage

Pin 9 must be set to a typical tuning voltage of 33 V (maximum 35 V and minimum 30 V). Alternatively, a constant current of 1 mA to 1.5 mA can also be applied. Figure 3 shows an alternative supply from a 140 V source. The zener diode prevents the tuning voltage at pin 9 from exceeding 33 V.

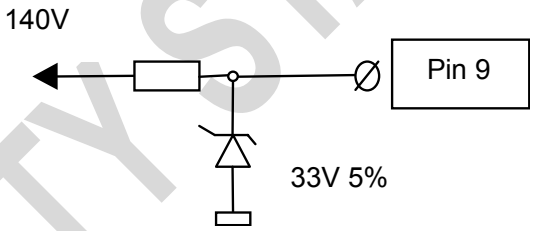

Fig 3. Tuning supply

11.5 IF bandwidth (3 dB)

The typical bandwidth is 12 MHz

11.6 IF output impedance

Measured at 36.15 MHz

- 37 + j54 Ω (asymmetrical)
- 87.6 + j21 Ω (symmetrical)

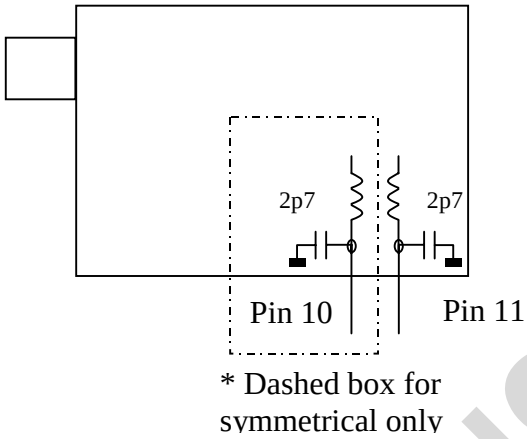

Fig 4. IF output impedance

11.7 I²C-Bus load

The UV1316 MK4 has a series resistor of 370 Ω and 370 Ω respectively in each of the SCL and SDA lines and a shunt capacitance of 18 pF to ground at the pins. A capacitive load of typically 56 pF is allowed at these pins for standard 100 kHz I²C bus mode.

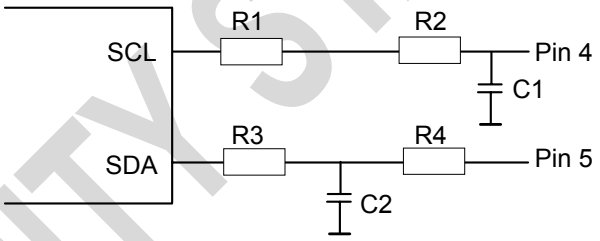

Fig 5. Internal I²C bus loading

11.8 IF load

The maximum permissible resistive load is 280 Ω, the maximum capacitive load is 40 pF

To guarantee optimum signal handling performance, the reactive load of the IF circuitry (interconnections, saw filter) has to be tuned to tuner IF center frequency according to the following formula

$$L_{tune} = \{(2 \cdot \pi \cdot f)^2 * (C_{int} + C_{stray} + C_{SAW})\}^{-1}$$

Where C_{int} = internal capacitance of the tuner
= 2.7 pF for asymmetrical
= 1.35 pF for symmetrical

C_{stray} = stray capacitance attributed to layout in the chassis

C_{SAW} = intrinsic capacitance of the SAW filter used/selected

f = desired IF frequency, usually centered between picture and sound

The IF output is to be maintained at 107 dBμV maximum. In case this limit is exceeded, the tuner gain should be reduced accordingly

11.9 Automatic gain control (AGC)

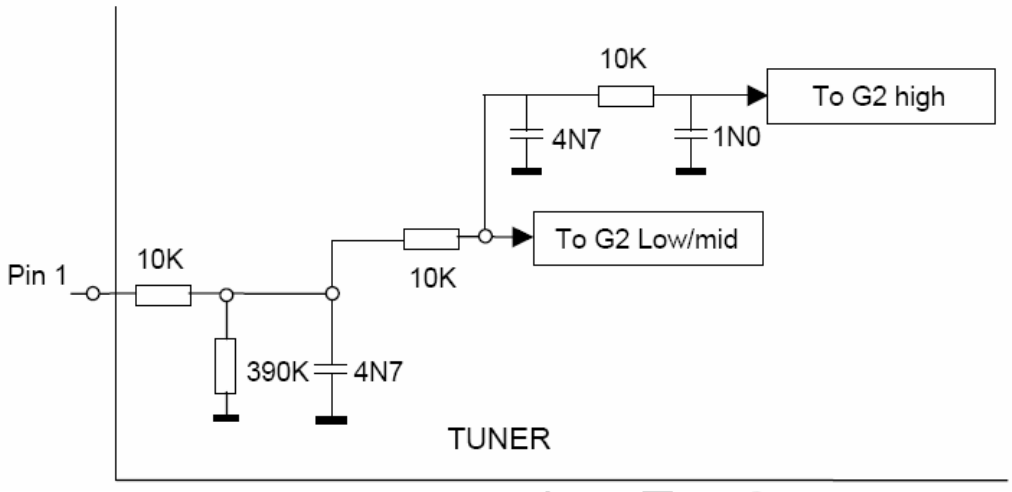

Fig 6. AGC connection

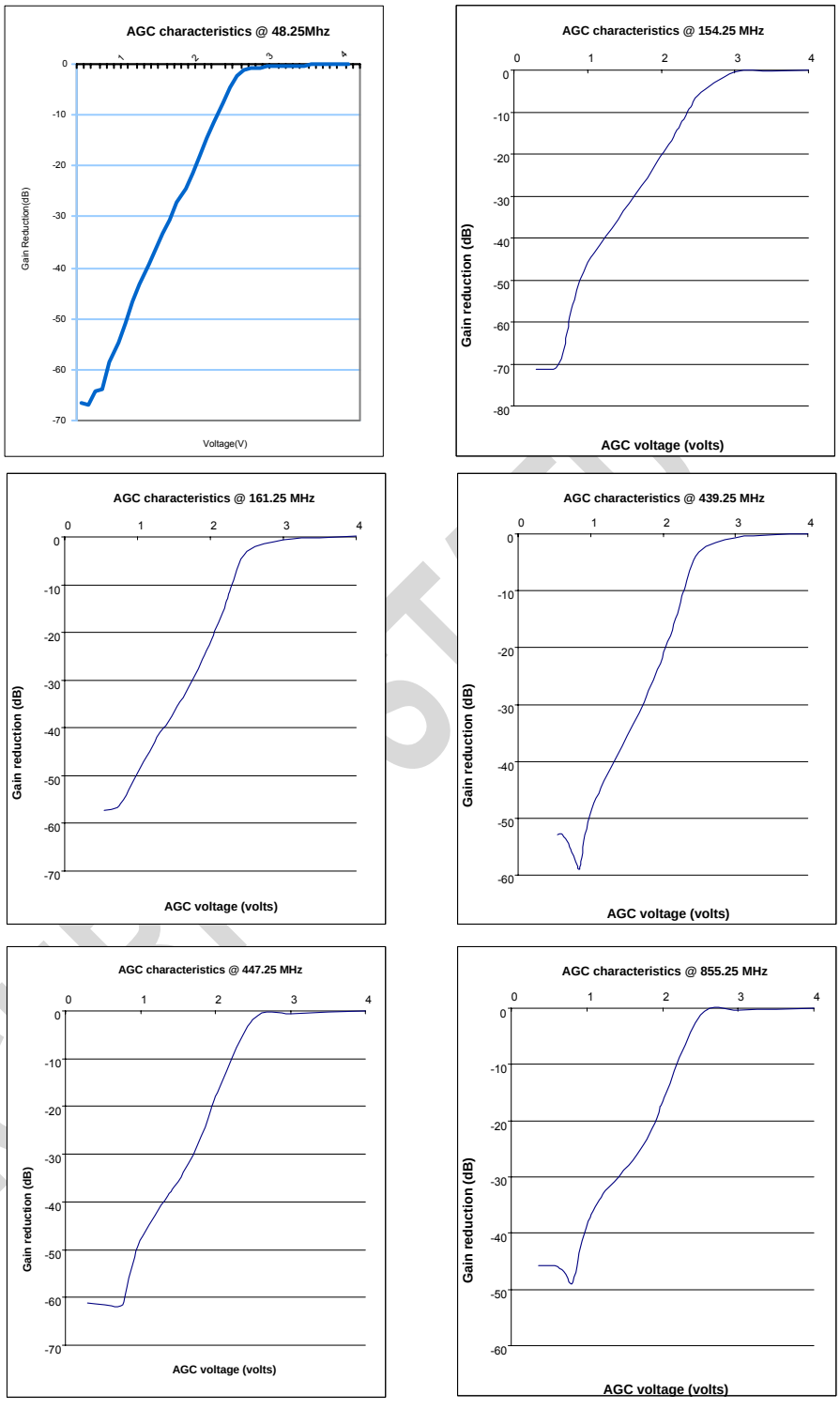

Fig 7. Typical AGC curves

12. Package outline

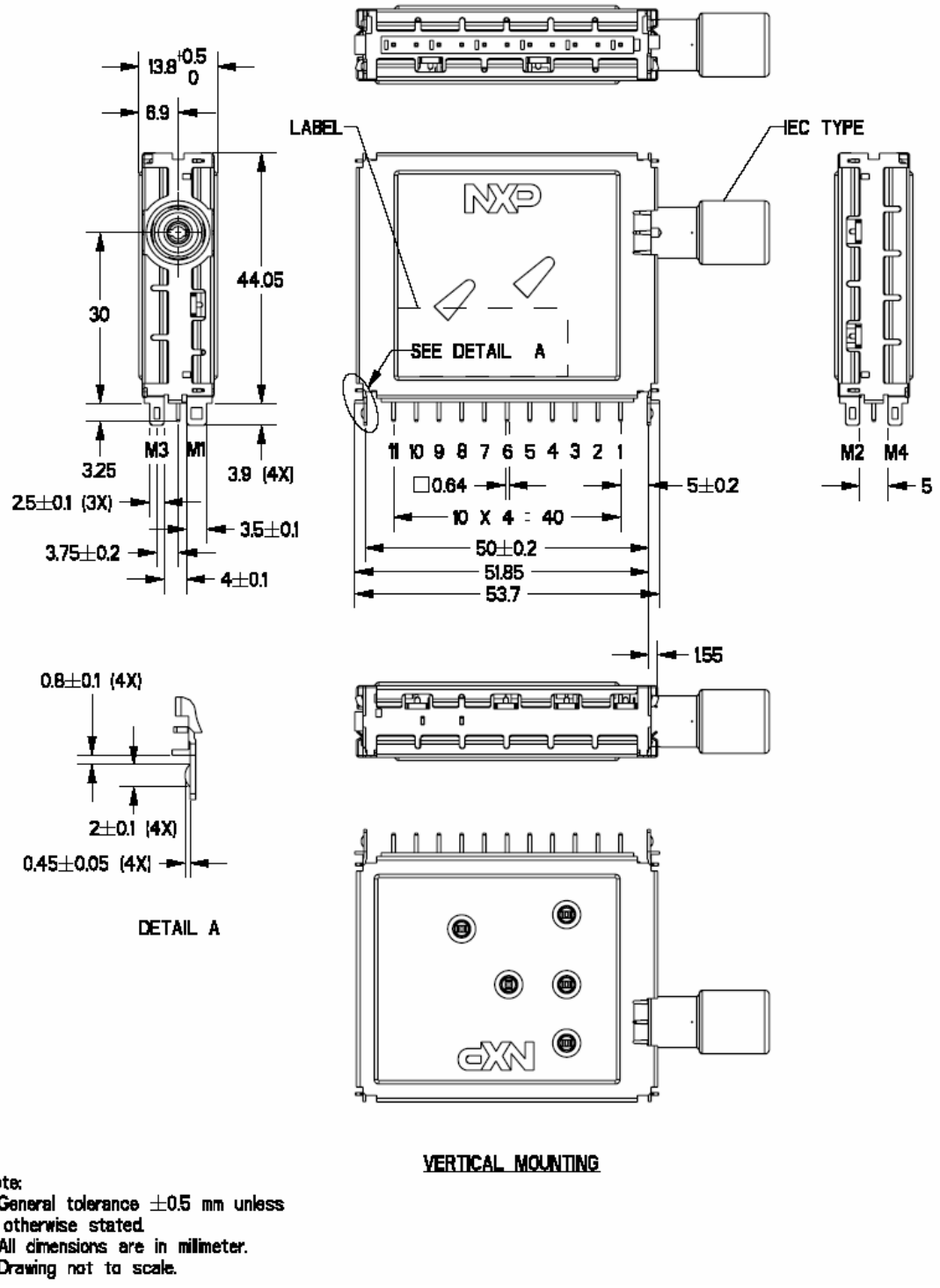

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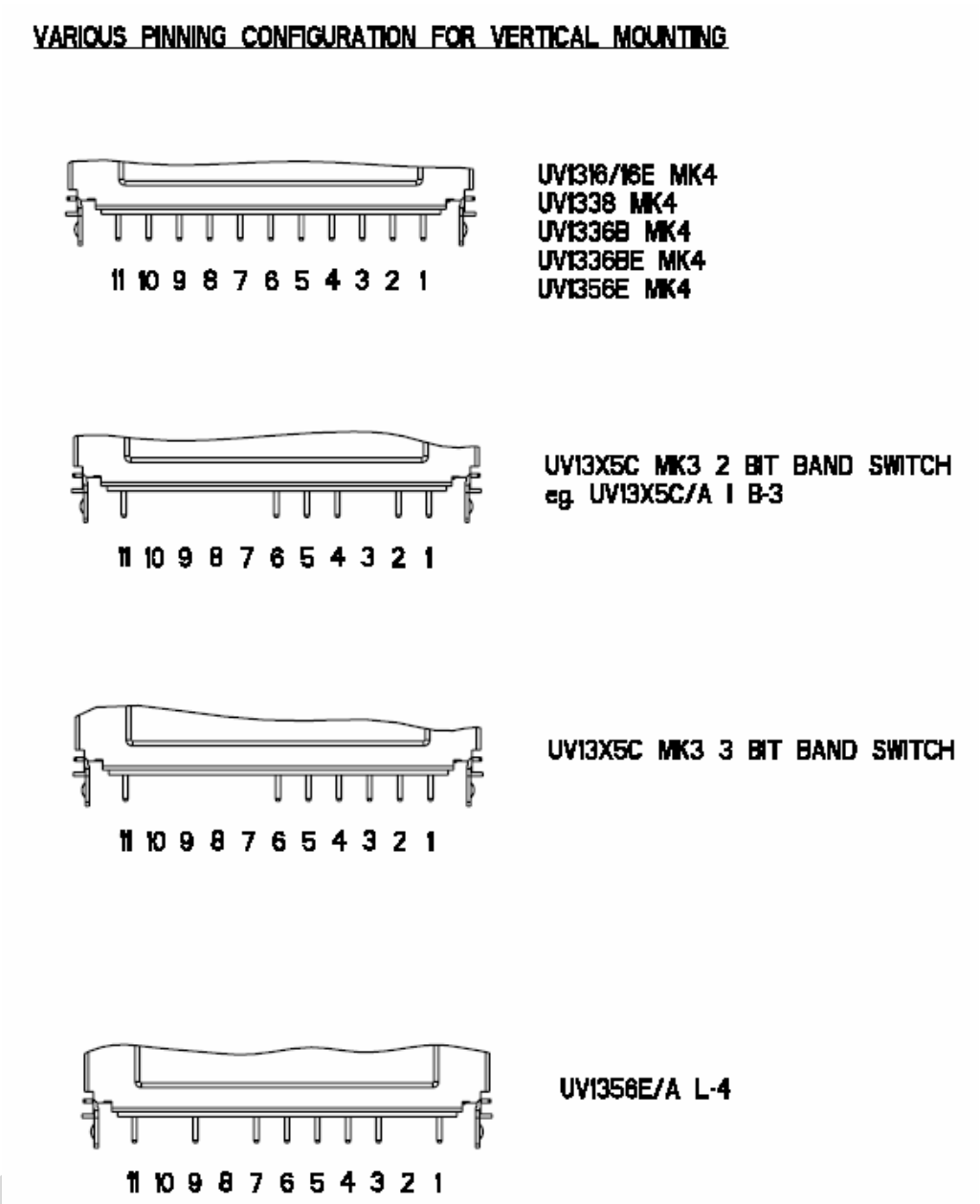
Fig 8. Package outline



(2) Product mechanics 3139 149 0157 – page 2 (date 2007-07-05)

Fig 9. Package outline

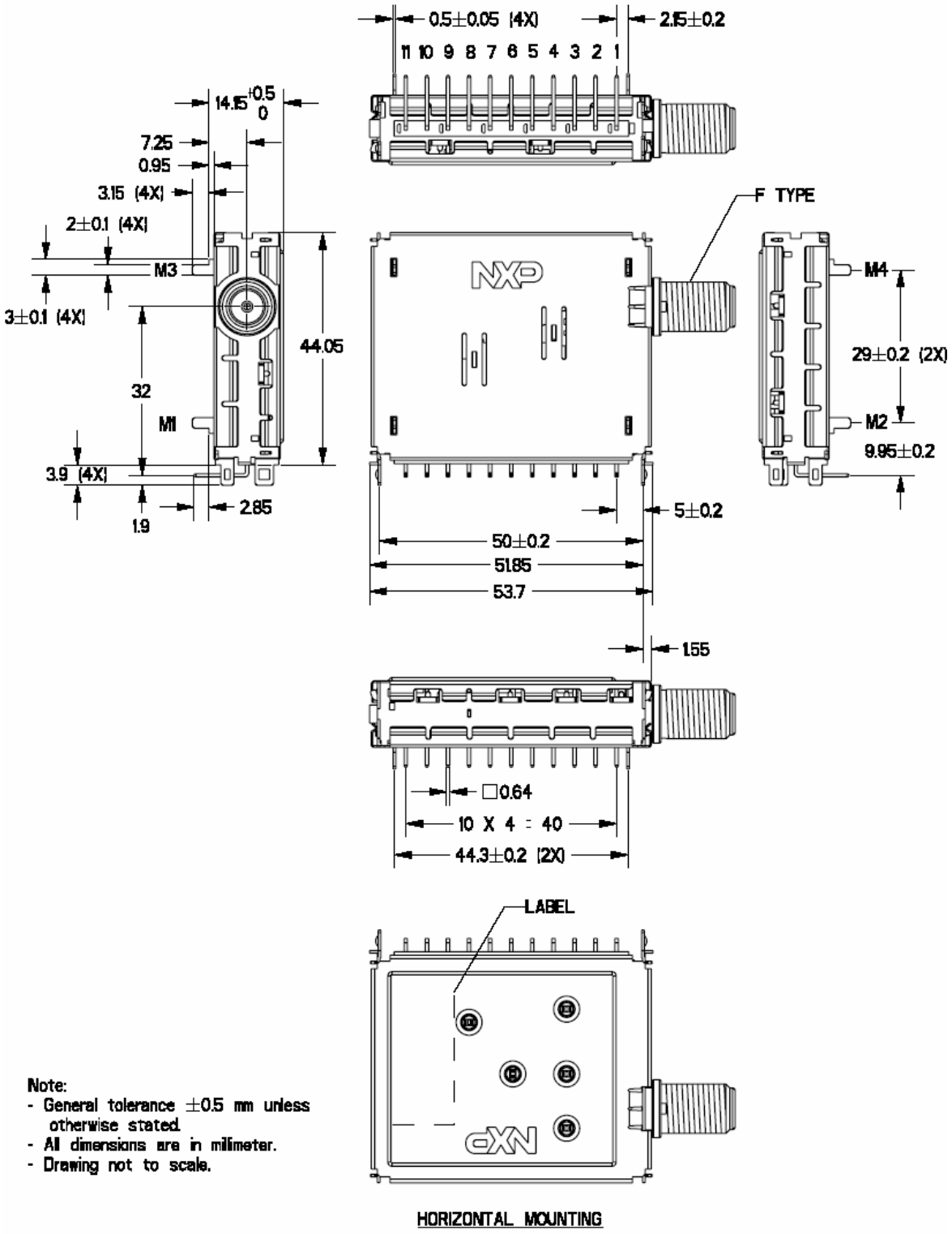


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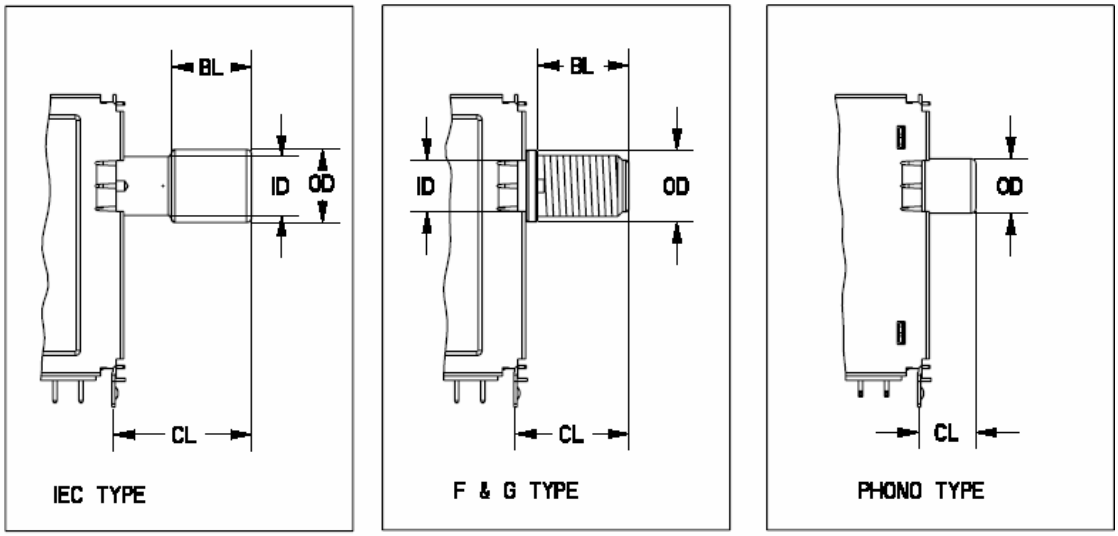
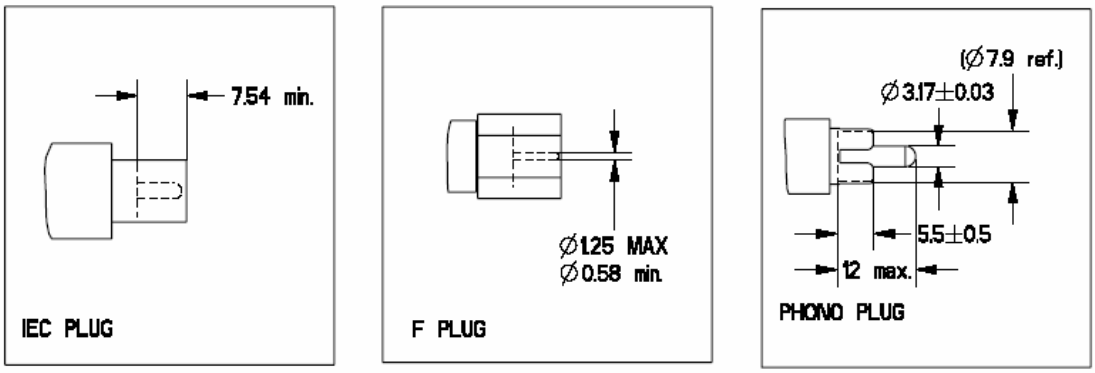
Fig 10. Package outline

AERIAL CONNECTOR TYPE



CONNECTOR TYPE	CONNECTOR LENGTH, CL	BODY LENGTH, BL	OVERALL DIAMETER, OD	INNER DIAMETER, ID
IEC-I	14.8±0.5	12.3±0.3	11.0±0.1	8.0±0.2
IEC-L	21.2±0.5	12.3±0.3	11.2±0.1	9.0±0.3
IEC-D	25.4±0.5	12.3±0.3	11.1±0.2	8.0±0.2
F-F	17.5±0.5	14.1±0.5	11.0±0.2	--
F-G	22.2±0.5	16.5±0.3	12.3+0/-0.3	9.8±0.2
PHONO-P	8.7±0.5	–	8.35+0/-0.1	--

MALE CONNECTOR REQUIREMENT



For dimension which is not reflected in drawing, refer to IEC 60169-2 (for IEC plug) and IEC 60169-24 (for F plug).

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Fig 11. Package outline

13. Packing information

The products are packed in the carton box and transferred to customers by Pallet Transport.

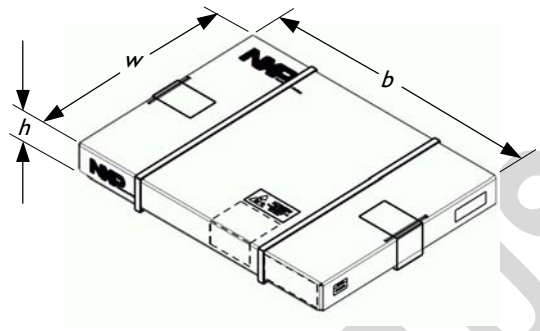

Fig 12. Example of Carton Box

Table 18. Package information

Carton boxes are made of corrugated fibreboard which is free of environmentally banned substances

Mounting type	Package	Dimension L x W x H (cm)	Number of sets	Gross weight (kg)
IEC-I vertical	Carton	46 x 34 x 7.5	98	3.79
	Pallet	120 x 105 x 105	7742	321.4
IEC-L vertical	Carton	46 x 34 x 7.5	98	3.62
	Pallet	120 x 105 x 105	7742	308.0
IEC-P vertical	Carton	46 x 34 x 8.2	98	3.91
	Pallet	120 x 105 x 105	7056	303.6
IEC-I horizontal	Carton	46 x 34 x 9.4	60	3.09
	Pallet	120 x 105 x 105	3900	222.9
IEC-L horizontal	Carton	46 x 34 x 9.4	60	3.12
	Pallet	120 x 105 x 105	3900	224.9

14. Mounting

14.1 Punching pattern of chassis PCB

For optimum mounting of the tuner to a PCB, the punching pattern is recommended

The tuner must be mounted without clearance between the tuner supporting surface and the printed circuit board (PCB). When mounted in this way, the tuner must be soldered to the PCB. This can be achieved by pressing the unit vertically onto the PCB during soldering

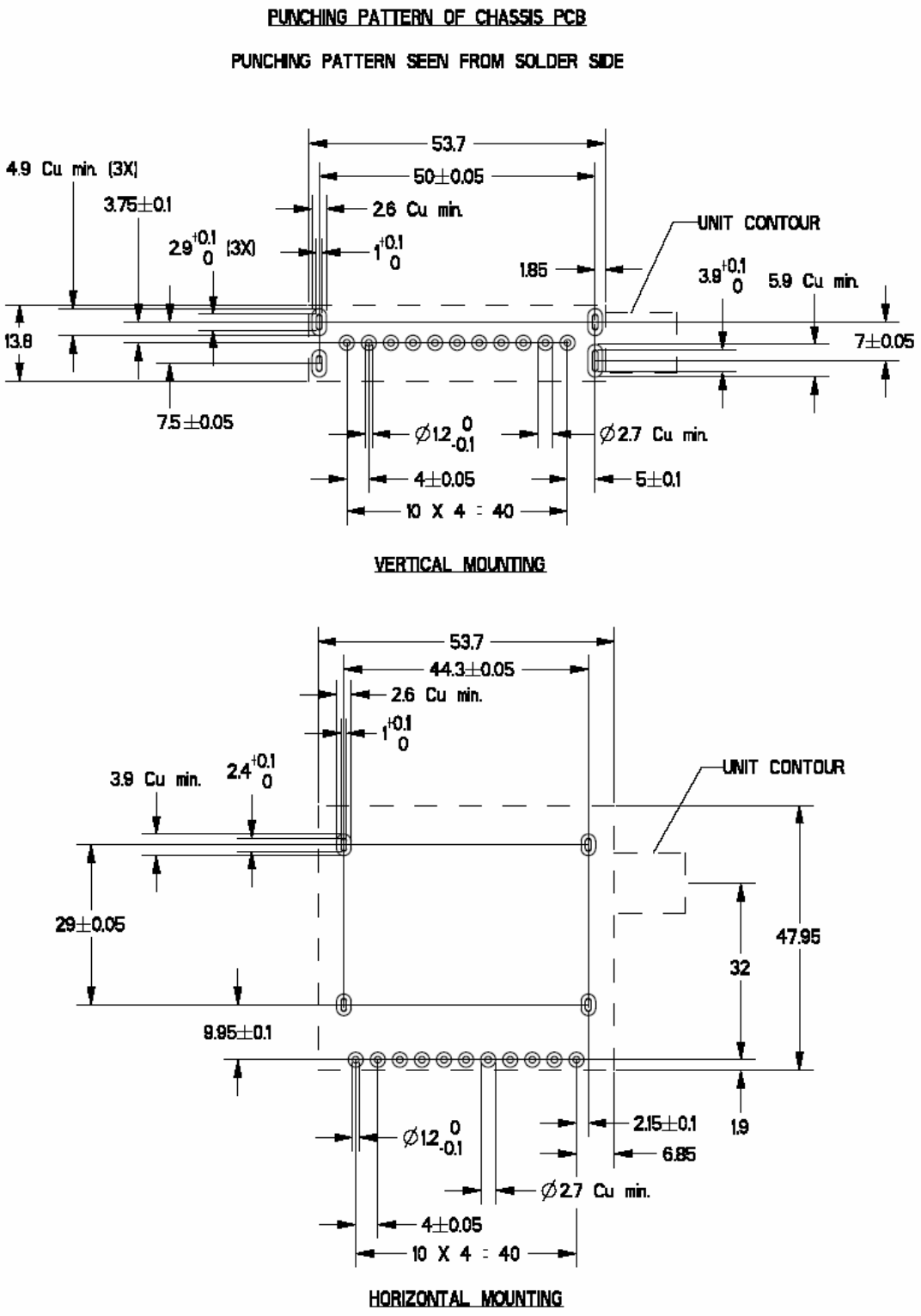

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Fig 13. Mounting

14.2 Aerial connections

Standard IEC socket female 75 Ω

14.3 Solderability

The solderability of pins and mounting tags when tested initially and after 16 hour steam ageing in accordance with “IEC 60068-2-20”, test TA, method 1 (solder bath 235 °C for 2 s), results in a wetted area of 95 %. No de-wetting will occur when soldered at 260 °C for 5 s.

14.4 Resistance to soldering heat

The product will not be damaged when tested in accordance with “IEC 60068-2-20”, test Tb, method 1A (solder bath 260 °C for 10 ± 1 s)

14.5 Mass

Approximately

- 34 g (IEC)
- 35 g (IEC long)
- 36g (IEC ultra long)

14.6 Robustness of pins

The pins will not be damaged when tested in accordance with “IEC 60068-2-21”

- Test Ua1, tensile of 10 N in axial direction
- Test Ua2, thrust of 4 N in axial direction

15. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UV1316_MK4	15-01-2003	Preliminary data sheet	-	-
Modification	• Draft created by Toh Yeow Teng			
UV1316_MK4	22-01-2003	Preliminary data sheet	-	15-01-2003
Modification	• Change in pg 6			
UV1316_MK4	03-03-2003	Preliminary data sheet	Rev a	22-01-2003
Modification	• Change in pg 2, 6, 7, 9 and last page			
UV1316_MK4	24-03-2003	Preliminary data sheet	Rev a	03-03-2003
Modification	• Change in pg 2, 6, 10 to 15			
UV1316_MK4	07-04-2003	Preliminary data sheet	Rev a	24-03-2003
Modification	• Change in pg 3, 6, 7 and 9			
UV1316_MK4	22-04-2003	Preliminary data sheet	Rev a	07-04-2003
Modification	• Change in pg 2, 6, 15, 16, 17 to 20			
UV1316_MK4	09-05-2003	Product data sheet	Rev b	22-04-2003
Modification	• Change from Preliminary to Product spec • Updating pg 2, 8, 9, 15 and 16			
UV1316_MK4	09-06-2003	Product data sheet	Rev c	09-05-2003
Modification	• Updating pg 6			
UV1316_MK4	10-09-2003	Product data sheet	Rev d	09-06-2003
Modification	• Updating Mechanical drawings			
UV1316_MK4	10-10-2003	Product data sheet	Rev e	10-09-2003
Modification	• Updating Mechanical drawings			
UV1316_MK4	12-01-2004	Product data sheet	Rev f	10-10-2003
Modification	• Pg 2 – update Ordering information • Pg 19 to 23 - update Mechanical drawings • Pg 26 – update RF solutions sales offices			
UV1316_MK4	04-02-2004	Product data sheet	Rev g	12-01-2004
Modification	• Pg 19 – update Packing info			

Document ID	Release date	Data sheet status	Change notice	Supersedes
UV1316_MK4	12-02-2004	Product data sheet	Rev h	04-02-2004
Modification	• Pg 2 – update Ordering information: add new type UV1316/A P-4 and UV1316/A L H-4 • Pg 20 to 24 - update Mechanical drawings			
UV1316_MK4	18-02-2004	Product data sheet	Rev i	12-02-2004
Modification	• Pg 3 – update Intermediate frequencies: system L' refer to note 2			
UV1316_MK4	23-02-2004	Product data sheet	Rev j	18-02-2004
Modification	• Pg 2 – update Ordering information: change description for UV1316/A P-4 • Pg 3 – update note 2: Does not cover channel FA			
UV1316_MK4	20-05-2004	Product data sheet	Rev k	23-02-2004
Modification	• Pg 20 to 24 - update Mechanical drawings			
UV1316_MK4	05-11-2004	Product data sheet	Rev l	20-05-2004
Modification	• Pg 2 – update Ordering information: add new type UV1316/S L-4 • Released into eMatrix systems			
UV1316_MK4	08-06-2005	Product data sheet	Rev m	05-11-2004
Modification	• Pg 2 – update Ordering information: add new type UV1316/A D H-4 • Pg 18 – update Packaging info • Pg 19 – update Mass • Pg 20 to 24 - update Mechanical drawings			
UV1316_MK4	27-06-2006	Product data sheet	Rev n	08-06-2005
Modification	• Pg 15 – correction of typo error			
UV1316_MK4	04-07-2007	Product data sheet	Rev o	27-06-2006
Modification	• Pg – update AGC characteristics : typical AGC curves 48.25 MHz • Update from Philips to NXP			

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification
Product [short] data sheet	Production	This document contains the product specification

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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